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SPECIFICATION

RADIATION SHIELDING DIE CARRIER PACKAGE

BACKGROUND OF THE INVENTION

1. Field Of The Invention

[0001] The present invention relates to a die carrier package. More particularly, the present invention relates to a radiation shielding die carrier package that protects a semiconductor die disposed therein from radiation contacting the die carrier package from any direction.

2. The Background Art

[0002] In the extreme environments where semiconductors may be used, it is imperative to shield the semiconductor die from radiation to ensure the reliability of the integrated circuits implemented in the semiconductor die.

[0003] Typically, an integrated circuit die is disposed in a plastic or ceramic package that provides little protection for the semiconductor die from radiation. Shielding that is applied to or incorporated into a plastic or ceramic package to

protect the semiconductor die from x-ray or other types of electromagnetic radiation is well known to those of ordinary skill in the art. There are problems, however, with the known shielding techniques employed to protect a semiconductor die disposed in a plastic or ceramic package from radiation. These problems include shielding that fails in difficult environments, shielding that does not protect the semiconductor die from every direction, and shielding that is either to cumbersome or expensive to include in the package.

[0004] Examples of prior art devices with these problems are disclosed in United States Patent No. 5,635,754, along with descriptions of numerous embodiments of packages designed to provide radiation shielding. Though numerous packages are described which include various amounts of shielding, none of the packages described will prevent radiation from all directions from entering the cavity in the package in which the semiconductor device is disposed. Each of the packages described includes either an insulating feedthrough for external leads or a plastic portion that will allow radiation into the package that is not otherwise blocked by additional shielding.

[0005] Programmable logic devices (PLD) are well known to those of ordinary skill in the art. A PLD typically includes uncommitted groups of digital logic, which may be programmed to form higher digital logic functions, and uncommitted routing channels, which may be programmed to connect together the

programmed digital logic. An example of a PLD is a field programmable gate array (FPGA). PLDs are often employed in applications where the implementation of an integrated circuit in a semiconductor die using mask programmed techniques is prohibitively expensive because the number of semiconductor dies produced is quite small. Some of the applications PLDs include use in military and aerospace hardware.

BRIEF DESCRIPTION OF THE INVENTION

[0006] According to the present invention, a semiconductor die carrier has a radiation shielding base with a radiation shielding integrated base flange having an upper surface extending orthogonally from an upper surface of the base. A substrate is disposed on said radiation shielding base and around said integrated base flange. An uppermost tier of the substrate has an upper surface that is not higher than the upper surface of said integrated base flange. A radiation shielding seal lid has a radiation shielding integrated seal lid flange with a lower surface disposed on the upper surface of the uppermost tier of said substrate. A semiconductor die is disposed in a cavity formed by the radiation shielding base and the radiation shielding integrated base flange, the semiconductor die has an upper surface that is not higher than the upper surface of said integrated base flange.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1A is a first cross section of a radiation shielding die carrier package according to the present invention.

[0008] FIG. 1B is a second cross section of a radiation shielding die carrier package according to the present invention.

[0009] FIG. 2 is a top-down view of a radiation shielding die carrier package according to the present invention.

[0010] FIG. 3 is a flow diagram describing the process of forming a radiation shielding die carrier package according to the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

[0011] Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

[0012] According to the present invention, a semiconductor die is disposed in a package that shields the semiconductor die from radiation particles in all directions. The shielding is provided in the package by a metal shielding material

employed to form a base for the package and a seal lid for the package. Both the base and the seal lid each have an integrated flange made from the same metal shielding material as the base and the seal lid. In the assembled package, the flange of the base and the flange of the seal lid are positioned so that surfaces at the end of the flanges are either at the same level or overlap one another slightly.

[0013] In this arrangement, the base protects the semiconductor die from radiation below, the seal lid protects the semiconductor die from radiation above and the flanges protect the semiconductor die from radiation on the sides. It will be appreciated by those of ordinary skill in the art that referring to the direction of radiation as being from above, below, and the sides with reference to the semiconductor package is only done to help the reader by providing a frame of reference. It should be well understood that these are merely relative terms such that above, below, and the sides are simply referencing first, second, third or fourth directions.

[0014] In FIG. 1A, a radiation shielding semiconductor die package 10 is illustrated in cross-section according to the present invention. The semiconductor die package 10 has a shielding metal base 12 upon which a semiconductor die 14 is disposed. The shielding metal base 12 has an integrated base flange 16 that extends orthogonally from the upper surface of the shielding metal base 12. The shielding metal base 12 and the integrated base flange 16 form a cavity for the

disposition of the semiconductor die 14. The integrated base flange 16 surrounds the semiconductor die 14, and is according to the present invention, at least as tall as the semiconductor die 14. Preferably, the integrated base flange 16 will have a height that is 0.05 mm greater than the height of the semiconductor die 14.

[0015] Disposed on the shielding metal base 12 and around the perimeter of the integrated base flange 16 is a substrate 18 formed from ceramic or other substrate materials well known to those of ordinary skill in the art. The substrate 18 has first and second tiers 20 and 22, respectively, on which electrically conductive tabs 24 are preferably disposed on an upper side of first and second tiers 20 and 22, respectively. A shielding metal seal lid 26 with an integrated seal lid 28 is disposed on the upper side of the second tier 22 of the substrate 18. The first and second tiers 20 and 22, respectively, each have first or vertical sides which face the outer side of the integrated base flange 16 and are oriented in the same direction as the integrated base flange 16, and second or upper sides which face the underside of shielding metal seal lid 26 and are oriented in the same direction as the shielding metal seal lid 26.

[0016] It should be appreciated according to the present invention that tiers in addition to first and second tiers 20 and 22, respectively, may be employed upon which are disposed electrically conductive tabs 24. When tiers in addition to first and second tiers 20 and 22, respectively, are employed according to the

present invention, the shielding metal seal lid 26 will be disposed on the uppermost additional tier.

[0017] A metal wire 30-1 is used to make an electrical connection from the semiconductor die 14 to the electrically conductive tab 24-1 disposed on first tier 20. The electrically conductive tab 24-1 is coupled to an electrically conductive path that traverses the substrate 18 through a first conductive via 32-1, a conductive line 34-1, and a second conductive via 36-1 connected to an external lead 38 disposed on a lateral portion 40 of the upper edge of the die carrier 10.

[0018] In FIG. 1A, a metal wire 30-1 is depicted that connects the semiconductor die 14 to an electrically conductive tab 24-1 on the first tier 20. Not shown in FIG. 1A is the connection of a metal wire 30 from the semiconductor die 14 to an electrically conductive tab 24 on the second tier 22. In order to depict such a connection, in FIG. 1B, a cross-section of the semiconductor die package 10 that is offset from the cross-section of the semiconductor die package shown in FIG. 1A is illustrated which depicts the connection of the semiconductor die 14 by a metal wire 30-2 to an electrically conductive tab 24-2 disposed on the second tier 22 of the substrate 18. The electrically conductive tab 24-2 is coupled to an electrically conductive path that traverses the substrate 18 through a first conductive via 32-2, a conductive line 34-2, and a second conductive via 36-2 connected to an external lead 38 disposed on a lateral portion 40 of the upper edge

of the die carrier 10. In an embodiment according to the present invention where additional tiers are employed, the electrically conductive tabs 24 disposed upon the additional tiers may be coupled to external leads 38 in a manner similar to that described for first and second tiers 20 and 22, respectively.

[0019] In FIG. 1A, it should be appreciated that the metal wire 30-1, the electrically conductive tab 24-1, the first conductive via 32-1, the conductive line 34-1, the second conductive via 36-1, and external lead 38 represent a plurality of metal wires 30-1, a plurality of electrically conductive tabs 24-1, a plurality of first conductive vias 32-1, a plurality of conductive lines 34-1, a plurality of second conductive vias 36-1, and a plurality of external leads 38. Further, in FIG. 1B, it should be appreciated that the metal wire 30-2, the electrically conductive tab 24-2, the first conductive via 32-2, the conductive line 34-2, the second conductive via 36-2, and external lead 34 represent a plurality of metal wires 30-2, a plurality of electrically conductive tabs 24-2, a plurality of first conductive vias 32-2, a plurality of conductive lines 34-2, a plurality of second conductive vias 36-2, and a plurality of external leads 38.

[0020] FIG. 2 illustrates according to the present invention an overhead view of the die carrier 10 without the shielding metal seal lid 26 depicted. In FIG. 2, the shielding metal base 12, the upper surface of the integrated base flange 16, the substrate 18, first and second tiers 20 and 22, respectively, electrically

conductive tabs 24-1 and 24-2, and external leads 38 disposed on lateral portions 40 of the upper edge of the die carrier 10 are illustrated.

[0021] In FIGS. 1A and 1B, the second tier 22, or the uppermost tier if more than two tiers are employed, is positioned so that the upper surface of the second tier 22 is not higher than the upper surface of the integrated flange 16. Preferably, the height of the second tier 22 is less than the height of upper side of the integrated base flange 16. When the height of the upper surface of the second tier 22 is equal to the height of the upper surface of the integrated base flange 16, the lower surface of the integrated seal lid flange 28 of the shielding metal seal lid 26 will also be positioned so that it is at the same height as the upper surface of the integrated base flange 16. In this manner, the lower surface of the integrated seal lid flange 28 is in the same plane as the upper surface of the integrated base flange 16.

[0022] When the height of the upper surface of the second tier 22 is preferably less than the height of the upper surface of the integrated base flange 16, the lower surface of the integrated seal lid flange 28 of the shielding metal seal lid 26 will be positioned lower than the height of the upper surface of the integrated base flange 16. In this manner, the integrated seal lid flange 28 will overlap the integrated base flange 16.

[0023] According to the present invention, the disposition of the integrated seal lid flange 28 and the integrated base flange 16 so the lower surface of the integrated seal lid flange 28 is either in the same plane as the upper surface of the integrated base flange 16 or that the integrated seal lid flange 28 overlaps the integrated base flange 16 prevents radiation from reaching the semiconductor die from the side of the die carrier 10.

[0024] In FIG. 3, a flow diagram describing the process of forming a shielding semiconductor die package according to the present invention is described. At step 100, a shielding metal base with an integrated base flange is machined according to any of several known techniques known to those of ordinary skill in the art.

[0025] The metal shielding material may be selected for its radiation shielding properties as desired. As is well known in the art, metals with a higher atomic weight, such as tantalum, tungsten or lead typically provide greater radiation shielding than metals with a lower atomic weight such as copper or aluminum. According to the present invention, the shielding material may be either a single atomic element or a combination thereof to provide the level of shielding desired for a particular application. Preferably, the shielding material employed in the base is copper tungsten (CuW), however, it will be appreciated by those of ordinary skill in the art that a variety of radiation shielding materials may

be used. Further, it is contemplated according to the present invention that radiation shielding materials that may be developed in the future that may be compatible with the structure of the present invention.

[0026] As described above, a substrate is disposed on the shielding metal base. Prior to this disposition, the substrate is first formed by any of several methods of manufacture well known to those of ordinary skill in the art. As an example of such a process of manufacture, a limited description of ceramic die carrier will be made herein. In this process, cut unfired flexible raw ceramic sheets, known to those of ordinary skill in the art as a green sheets, are processed as will be described and then stacked one on top of another and laminated to bond the green sheets together and thereby form the unitary body of the die carrier.

[0027] At step 102, a green sheet has a recess for the die carrier and the vias punched out, and at step 104, the via holes are filled with an electrically conductive material, preferably tungsten (W).

[0028] At step 106, as the die carrier is being built up from bottom to top, the electrically conductive materials that are disposed horizontally in the die carrier are screen printed as desired on the upper surface of the green sheets. The electrically conductive screen printed material is preferably tungsten (W). The horizontally disposed electrically conductive materials include the electrically

conductive tabs disposed on the first and second tiers, the external bond terminals disposed either in recesses on the lateral edges of the die carrier or on the lateral edges of the top of the die carrier and the electrically conductive lines connecting the electrically conductive tabs to the external bond terminals.

[0029] At step 108, after the green sheets have been laminated, back end processing steps occur which include shaping, cofiring, nickel plating, metal pad assembly, brazing, finish plating, snap breaking and edge grinding. Each of these steps and others well known to those of ordinary skill in the art will not be described herein to avoid overcomplicating the disclosure and to thereby obscure the present invention.

[0030] At step 110, the finished substrate is loaded into an alignment tool, and a silver copper (AgCu) braze material is applied to a portion of the substrate that will be attached to the shielding metal base. The shielding metal base is then also loaded into the alignment tool and affixed to the substrate by brazing in a cofire furnace. The shielding metal base is then nickel and gold plated.

[0031] At step 112, the semiconductor die is the disposed within the cavity on the shielding metal base formed by the integrated base flange.

[0032] At step 114, the semiconductor die is wired to the conductive tabs by any of several methods well known to those of ordinary skill in the art.

[0033] At step 116, the shielding metal seal lid with an integrated seal lid flange is machined according to any of several known techniques known to those of ordinary skill in the art. After machining the shielding metal seal lid is nickel and gold plated, and a layer of AuSn is applied to the lower surface of the integrated seal lid flange.

[0034] The metal shielding material may be selected for its radiation shielding properties as desired. As is well known in the art, metals with a higher atomic weight, such as tantalum, tungsten or lead typically provide greater radiation shielding than metals with a lower atomic weight such as copper or aluminum. According to the present invention, the shielding material may be either a single atomic element or a combination thereof to provide the level of shielding desired for a particular application. Preferably, the radiation shielding material employed in the shielding metal seal lid is CuW, however, it will be appreciated by those of ordinary skill in the art that a variety of radiation shielding materials may be used. Further, it is contemplated according to the present invention that radiation shielding materials that may be developed in the future that may be compatible with the structure of the present invention.

[0035] At step 118, the shielding metal seal lid is disposed on the substrate, and put into a furnace with a nitrogen gas ambient to affix the shielding metal seal lid to the substrate. The adhesion of the shielding metal seal lid to the substrate is due to the layer of AuSn applied to the lower surface of the seal lid flange.

[0036] While the invention has been described with reference to an exemplary embodiment, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.